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DIGITAL TV RESEARCH LINE

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1.- Introduction

In the last years, big changes are taking place in the digital TV due, among other reasons, to the arising of new encoding standards, allowing the High Definition TV (HDTV), the Scalable Video Coding (SVC), the Three Dimension TV (3DTV) or the Multi View coding (MVC) for Multi View TV. The computational cost of the video encoding and decoding tasks in these new scenarios is very large and demands new solutions based on more complex devices. In this context, the research on efficient implementations of encoders and decoders for embedded systems poses a big challenge.

GDEM has been researching for more than 15 years in digital TV and video coding related issues. In the last years, our group has been focused on real time video and audio encoders and decoders using latest generation DSPs. This research has been outlined in section 2. Now, we are working on two lines: scalable video decoding and 3DTV; these lines are outlined in section 3. Also, GDEM is committed to open a new research line in which multicore DSPs are intended to be used; this line is explained in section 4.

2.- Previous research

In the last years, GDEM has been working in speed optimization of software to be used in real time implementations of audio and video encoders/decoders based on latest generation DSPs. An optimization methodology has been developed. PC code has been used as a starting point, either the coding standard reference software or any other open code. This code is ported to the DSP and successive optimization steps are taken place until real time operation is reached. These work have been published in several conferences and journals [1][2][3].

As an additional result, an IP-STB has been developed and implemented over an in –house designed prototype (see Fig. 1-a) and also over a commercial prototyping board (see Fig. 1-b). This IP-STB can decode video encoded with different standards and has been used to carry out real-time tests on actual environments.

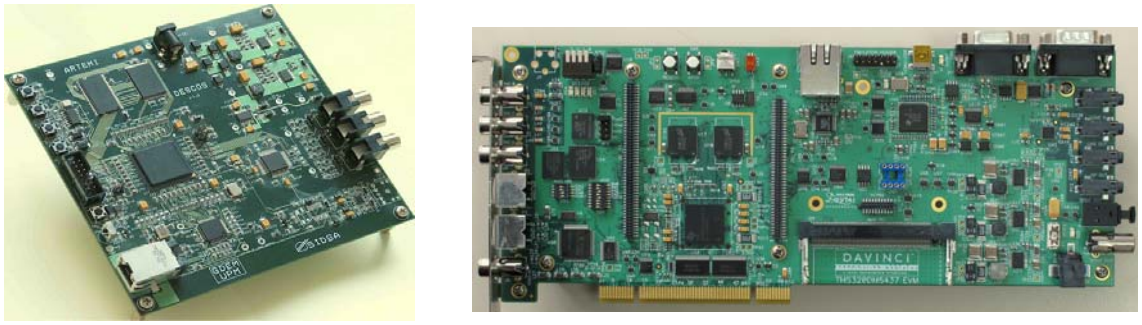

Fig. 1. IP-STB implementation a) over a GDEM designed board and b) over a comercial prototyping board.

As an example, Fig. 2 shows a testbench based on the IP-STB. From right to left, the picture shows a PC-based commercial H.264 encoder, a DVD player and the STB prototype, that is generating the video on the TV set.

At this time, the implementations we have been developing work in real time for SD. Now, the digital TV formats are evolving towards HDTV. The computational load of HDTV may be up to 5 times the one needed to support just SD, that is very far from the capacity of the modern DSPs (without specific embedded encoders/decoders).

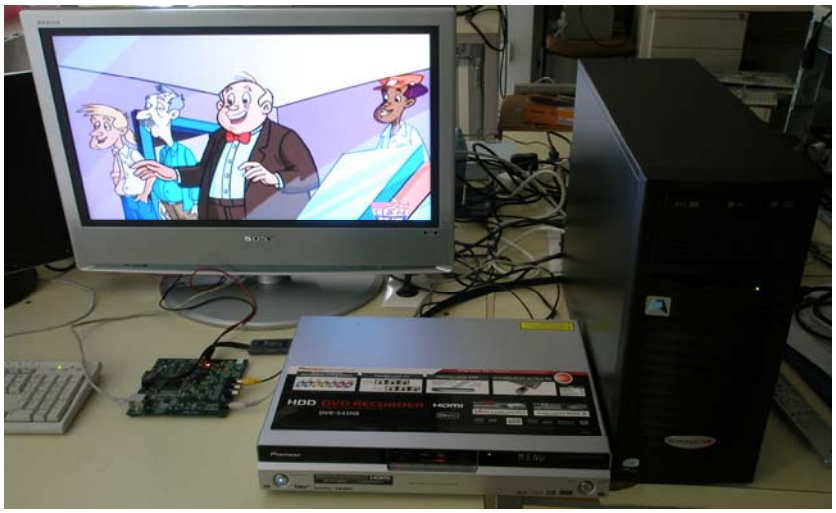

Fig. 2. Testbench to carry out real-time tests with video encoders/decoders.

3.- Current research

3.1. Scalable decoders

In the last years, the use of portable devices to play multimedia content has been continuously increasing. Such a multimedia content usually produce a large energy consumption, thus limiting the terminal operational time.

In this context, GDEM research focuses on the optimization of power/energy consumption for multimedia portable terminals by degrading the user quality of experience in order to increase the operational time.

To test the results of our research, we use a portable terminal based on a device with power consumption control capabilities, as well as a video coding standard that supports the quality degradation. In one hand, the beagleBoard [4] development platform (see Fig. 3) is used to implement the portable terminal. This platform is based on the OMAP3530 [5] multicore device (with an ARM GPP and a C64+ based DSP), that dinamically allows to change the clock frecuency and the power supply to adapt the power consumption to the computational load. In the other hand, a scalable video decoder will be used that allows to choose which parts of the stream are decoded at a time in function of the expected quality of experience.

Now, GDEM is working on the speed optimization of an scalable video decoder [6] (Open SVC[1] decoder [7]) running on the DSP within the OMAP3530 [8][9][10]. Up to now, the obtained results allow real-time operation with CIF sequences. Nevertheless, real-time decoding with largest formats will be very difficult, because of the complexity of the decoder algorithm, if only one DSP is available.

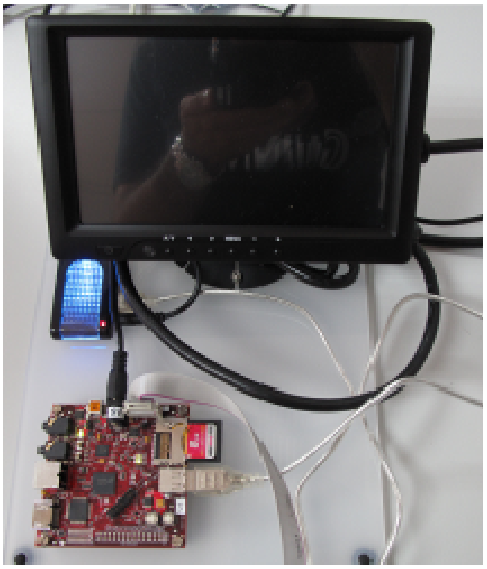

Fig. 3. Tarjeta Beagle Board

3.2. 3DTV

Recently, 3DTV has come on the scene. In this context, new video encoding and decoding algorithms will be employed [11]. These algorithms will be more complex and thus the encoders/decoders will have to support a large computational load.

To work with this new TV format, GDEM has being developing a complete testbench to capture, encode, transmit, decode and play 3D contents in actual environments. In Fig. 4, a block diagram of the testbench is shown. Also, several testbench pictures are shown in Fig. 5.

The testbench has two analogue video cameras whose outputs are digitized by two PC-based video capture boards. The PC runs also an in-house designed video encode, that mixes the left-eye and the right-eye images, encodes them with H.264 and transmits them as IP packets through an Ethernet network. This stream can also be modulated with DVB-T in order to be broadcasted. The receiver may consist of a DVB-T regular HD STB or an HD IP-STB, both connected to a 3D TV set, or a PC with a 3D compatible display and graphic card.

Now, this testbench is implemented at GDEM lab with state of the art components, which allows carrying out tests of the overall transmission chain. In the future we intend to change

[1] Currently GDEM works with the *Institut d'Electronique et de Télécommunications* of Rennes University (IETR)/ INSA Rennes in the development and optimization of the OpenSVC decoder (http://sourceforge.net/projects/opensvcdecoder/)

several elements with our own implementations of new 3D video coding standards, such as H264/MVC or the *freeview point encoder*.

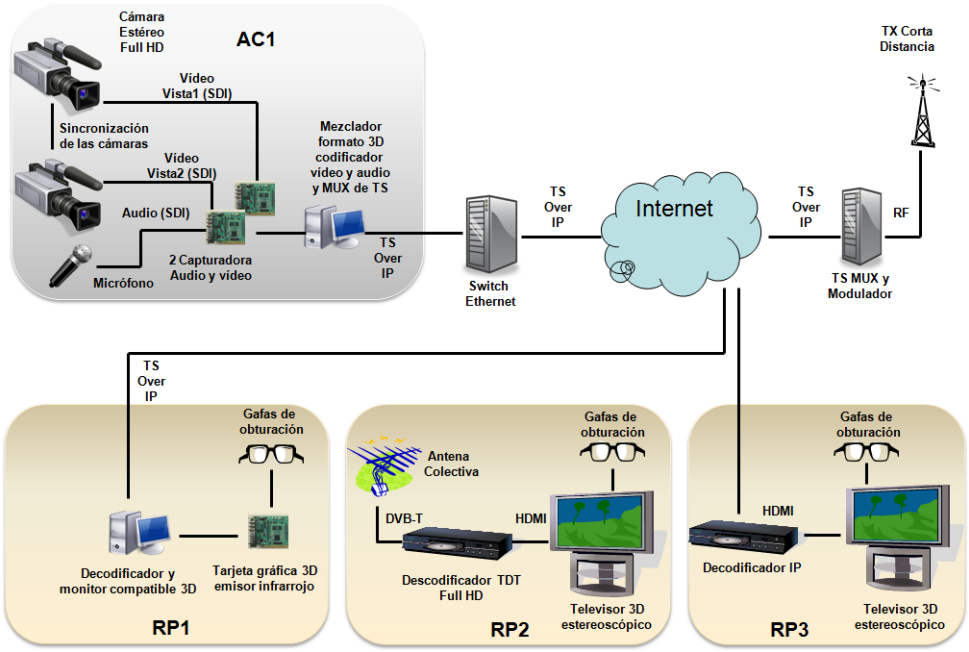

Fig. 4. Block diagram of the 3D TV testbench at GDEM lab

Fig. 5. Some testbench components

4.- Research on multicore based decoders

The increase in computational load associated with the HDTV or TV3D does not allow achieving real time solutions using implementations based on only one DSP. For example:

- In the reference [2] an H.264 decoder for Standard Definition (SD) using about 90% of the computational load of a DM6437 was presented. Therefore, the computational load of 5 DSPs should be used to decode High Definition sequences.

- In the reference [8] an SVC decoder for CIF sequences with 6 layers was presented using about 90% of the CPU. To decode High Definition sequences, the computational load of 20 DSPs should be used.

- In several papers the computational load of a MVC decoder has been analyzed. It increases the computational load of an H.264 decoder in about 30%. Therefore the computational load of 7 DSPs is required.

Moreover, in the coming months, the first release of the new standard HEVC [12] (also called H.265) will be published. This standard will reduce the stream bitrate in 50% respect H.264. The computational load of the encoder or decoder will be probably higher than required by the previous standards. Therefore this encoder/decoder could not be integrated in a single DSP.

Using the previous examples, it is obvious that is not possible to implement the new algorithms in a single DSP, so it is necessary to research in new solutions for the implementations of these algorithms. An interested option to increase the computational power maintaining the flexibility of the DSP solutions is to use multicore DSPs [13][14]. The research will be focused in the implementation of video decoders in multicore DSP.

Different video decoders will be implemented in this research topic using multicore DSP:

- H.264 for HDTV
- H.264 SVC
- H.264 MVC forTV3D
- HEVC

The starting point will be the reference SW from the standard or other freeware implementation for PC. The research will be focused in the decoder porting to the DSP development environment and the optimization of this SW for the multicore platform. Using the test-benchs described in previous sections, the implemented decoders will be test in actual situations.

In the annex II a relation of conferences and journals used to publish the results of the research is presented.

Annex I. References.

[1] F. Pescador, C. Sanz, M.J. Garrido, E. Juárez and D. Samper. “A DSP Based H.264 Decoder for a Multi-Format IP Set-Top Box”. IEEE Trans. on Consumer Electronics Vol. 54, Issue 1, Feb. 2008 pp. 145-153.
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[6] Joint Scalable Video Model JSVM-19, ISO/IEC JTC1/SC29/WG11 ITU-T SG16 Q.6, N9212, 2010
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[10] F. Pescador, D. Samper, M.J. Garrido, E. Juárez and M. Blestel. "A DSP based SVC IP STB using Open SVC Decoder". Int. Symposium on Consumer Electronics. Braunschweig Germany, 7-10 June 2010.
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[12] http://www.h265.net/category/news
[13] http://focus.ti.com/paramsearch/docs/parametricsearch.tsp?family=dsp&sectionId=2&tabId=2710&familyId=1995&paramCriteria=no
[14] http://focus.ti.com/paramsearch/docs/parametricsearch.tsp?family=dsp&sectionId=2&tabId=2274&familyId=1635&paramCriteria=no

Annex II. Conferences and Journals.

The most significant conferences in this area are:

- International Symposium on Low Power Electronics and Design
- DATE (Design Automation and Test in Europe)
- FPL (Field Programmable Logic)
- RSP (Rapid System Prototyping)
- ITC (International Test Conference)
- ISCAS (IEEE International Symposium on Circuits and Systems)
- ICIP (IEEE International Conference on Image Processing)
- SOCC (IEEE International SOC Conference)
- ICCE (IEEE International Conference on Consumer Electronics)
- ISCE (IEEE International Symposium on Consumer Electronics)
- ISSS+CODES (IEEE International Symposium on System Synthesis and HW/SW Codesign)
- DSD (Euromicro Conference on Digital System Design)
- DSP (Digital Signal Processing)
- MMEDIA
- Mobility
- Mobimedia

The journals with a higher impact factor in this area are:

- IEEE Transactions on VLSI Systems
- IEEE Transactions on CAD
- IEEE Transactions on Circuits and Systems for Video Technology
- IEEE Transactions on Circuits and Systems
- IEEE Transactions on Consumer Electronics
- IEE Electronics Letters
- ETRI Journal
- IET Proceedings on Computers and Digital Techniques